

REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested. Since the present Response raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested under the provisions of 37 C.F.R. §1.116.

Before addressing the specific grounds of rejection, Applicants take this opportunity to note the cancellation of Claims 7-9, 22 and 23. Applicants have cancelled Claims 7-9, 22 and 23 to reduce the number of issues for appeal in advancing the patentability of Claim 1. Applicants reserve the right to file one or more continuations to Claims 7-9, 22 and 23. Turning to the present grounds of rejection.

The specification stands objected to as allegedly failing to provide proper antecedent basis for the claimed subject matter. Claims 1, 2 and 4-9 stand rejected under 35 U.S.C. § 112, first paragraph, for allegedly failing to comply with the enablement requirement. Claim 9 is further rejected under 35 U.S.C. § 112, second paragraph, for allegedly failing to comply with the written description requirement. Claims 1, 2, 4-9, 22 and 23 stand rejected, under 35 U.S.C. § 103, for allegedly being unpatentable over U.S. Patent No. 6,749,527 to Xiang et al. ("Xiang et al.") in view of Applicants' Admitted Prior Art (AAPA) and U.S. Patent No. 6,432,802 to Noda et al. ("Noda et al."). Applicants traverse the aforementioned rejections and submit the following.

Referring first to the objection to the specification, the Examiner alleges that "the specification fails to provide support for the impurity of group IV, i.e, Pb, Sn and C, can form

dopant type in the semiconductor material.” Applicants submit that support for group IV dopants as a dopant implant for blocking threading defects is found in paragraphs 0022-0025 of Applicants’ specification.

Turning to the § 112 rejections, referring to MPEP 2164, Applicants submit that the essential goal of the enablement requirement is to clearly convey the information that an applicant has invented the subject matter which is claimed without undue experimentation.” *In re Barker*, 559 F.2d 588, 592 n.4, 194 USPQ 470, 473 (CCPA 1977). Such a review is conducted from the standpoint of one of skill in the art at the time the application was filed. *See e.g. Wang Labs v. Toshiba Corp.*, 993 F.2d 858, 865, 26 USPQ 2d 1767, 1774 (Fed. Cir, 1993). Information, which is well known in the art, need not be described in detail in the specification. *See Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1379-1380, 231 USPQ 81, 90 (Fed. Cir. 1986).

Referring to page 3 of the Final Office Action, the Examiner states the following:

“with respect to claim 1, claim 1 recites: “a first strain layer of semiconductor material doped of a first dopant type located on a substrate....a peak concentration of blocking impurity dopants materials selected from *group consisting of In, Pb, Sb and Sn*...”. Among the four dopant materials listed above only In and Sb are well known in the art to form a conductivity type in the semiconductor material 110/120. What is the dopant type formed by Pb or Sn?”

It appears that the Examiner is considering the terms “first dopant type” and “blocking impurity dopant” as recited in Claim 1 to be referring to the same dopant for the same purpose. This interpretation is incorrect and is inconsistent with the specification as read by one of ordinary skill in the art. Referring to Claim 1 and paragraph 0021 of Applicants’ specification, the terms “first type dopant” and “second type dopant” as used to describe the dopants of the channel region and the source and drain regions of the substrate as interpreted by those skilled in the art

means a conductivity type, i.e., p-type or n-type. Applicants describe one embodiment in paragraph 0021 of Applicants' specification, in which the source and drain regions are n-type doped and the region of the substrate between the source and drain regions is doped with a p-type dopant. As known by one of ordinary skill in the art, the doping of the source and drain regions classify the conductivity type, i.e., n-type or p-type, of the device. The conductivity type reflects whether the majority charge carriers of the device are electrons, as in n-type conductivity devices, or holes, as in p-type conductivity devices.

Contrary to the first type dopant and the second type dopant, the "blocking impurity dopant" is not an impurity that defines the conductivity type of the device, but instead impedes the growth of threading defects. Examples of blocking impurity dopants are illustrated in paragraphs 0022 to 0025 of Applicants' specification. There is no requirement that the blocking impurity dopants be classified as a p-type or n-type dopant, since the function of the blocking impurity dopants is to reduce the propagation of defects and is not to determine the majority charge carriers of the device.

In light of the above, Applicants have complied with the enablement requirement. Applicants' respectfully submit that the 35 U.S.C. § 112, first paragraph, rejection of Claims 1, 2 and 4 has been obviated. Claim 9 has been cancelled. Applicants respectfully request that the § 112, first paragraph, rejections be withdrawn.

In the event that the Examiner maintains this enablement rejection, Applicant respectfully requests, in accordance with the principles of compact prosecution, that the Examiner articulate, on the record and with specificity sufficient to support a prima facie case of non-enablement, the factual basis on which it is alleged that it would be beyond

the level of ordinary skill in the semiconductor art to make and use the claimed invention without undue experimentation. (MPEP §2164.01).

Applicants have also cancelled Claim 7. In light of the cancellation of Claim 7, Applicants submit that the § 112, second paragraph, rejection has been obviated and respectfully request withdrawal thereof.

Turning to the § 103 rejections, to establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art. *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Xiang et al. fails to render Applicants' claimed structure unpatentable, because Xiang et al. fails to teach or suggest each and every limitation of Claim 1. Specifically, Xiang et al. fails to teach or suggest a semiconductor field-effect transistor device that includes a peak concentration of blocking impurity dopant materials selected from the group consisting of In, Pb, Sb and Sn located substantially at an interface between a first strained layer of semiconductor material and a SiGe substrate, wherein the blocking impurity dopant materials partially or fully occupy each of the one or more threading dislocations, misfit dislocations or crystal defects at the interface and substantially inhibit diffusion of the implanted source and drain dopants from diffusing along the threading dislocations, misfit dislocations or crystal defect along the interface, as recited in Claim 1.

Xiang et al. does not teach or suggest blocking impurity dopant materials that occupy one or more threading dislocations, misfit dislocations or crystal defects. Xiang et al. discloses a structure in which the mobility of a strained silicon layer is augmented through incorporation of carbon into a strained silicon lattice to which strain is also imparted by an underlying silicon

germanium layer. To provide the strain augmentation, Xiang et al. discloses a carbon implant into silicon, which fails to teach or suggest a peak concentration of blocking impurity dopant materials selected from the group consisting of In, Pb, Sb and Sn, in which the implant is located substantially at an interface between a first strained layer of semiconductor material and a SiGe substrate, wherein the blocking impurity dopant materials partially or fully occupy each of the one or more threading dislocations, misfit dislocations or crystal defects at the interface, as recited in Claim 1.

Referring to page 6 of the Final Office Action, the Examiner states:

“The blocking impurity dopant material of Xiang et al. comprises halo regions (first dopant type) implanted using low energy at a small angle, to suppress short channel throughput. Moreover, Xiang et al. does use a neutral species, carbon, for the same intended purpose. Thus, Xiang is shown to teach all the features of the claim with the exception of explicitly disclosing the peak concentration is located substantially at the interface; and utilizing In, Pb, Sb and Sn for the blocking impurity materials.”

Applicants respectfully disagree. First, the halo regions disclosed in Xiang et al. are for reducing diffusion of dopants, i.e., transient diffusion that occurs during annealing, from the source and drain regions. Second, there is no disclosure of using carbon (C) as a halo dopant as alleged by the Examiner. Third, the carbon implant disclosed in Xiang et al. is for reducing the lattice dimensions of the semiconductor layer that is being implanted with carbon relative to the underlying substrate material. Implanting to modify lattice structure of the substrate is differentiated from implanting to stop diffusion of other dopants through the substrate, in which implanting to reduce source and drain dopant diffusion is the function of halo implants. To summarize, the implantation steps disclosed in Xiang et al. do not introduce blocking impurity dopant materials that occupy one or more threading dislocations, misfit dislocations or crystal

defects, as recited in Claim 1. Further, as noted by the Examiner on page 6 of the Final Office Action, Xiang et al. does not teach or suggest blocking impurity dopant materials selected from the group consisting of In, Pb, Sb and Sn, as recited in Claim 1.

Noda et al. fails to fulfill the deficiencies of Xiang et al. Noda et al. provides a method of fabricating a semiconductor structure in which an amorphous layer is formed into a semiconductor region by implanting heavy ions with a large mass using a previously formed gate electrode as an ion implantation mask. Applicants observe that in Noda et al. substrate 100 is shown as a single material. As such, Noda et al. does not teach or suggest a structure including a strained semiconductor layer located atop a substrate in which an interface is present between the two material layers. Since no interface is present between a strained semiconductor layer and an underlying substrate within Noda et al., the applied reference cannot and does not teach or suggest a structure in which a peak concentration of blocking impurity dopant materials from the group consisting of In, Pb, Sb and Sn is located substantially at the interface, wherein the blocking impurity dopant materials partially or fully occupy each of the one or more threading dislocations, misfit dislocations or crystal defects at the interface and substantially inhibit diffusion of the implanted source and drain dopants from diffusing along the threading dislocations, misfit dislocations or crystal defect along the interface, as is positively recited in the claims of the present application.

Referring to Page 6 of the Final Office Action, Applicants observe that the Examiner relies on the halo implants within Noda et al. for allegedly teaching utilizing the use of In, Pb, Sb and Sn. Applicants submit in this regard that In, Pb, Sb and Sn are used to form halo implants that are located within a doped layer 103 of semiconductor substrate 100 as provided in Noda et

al. After annealing, the halo implants are activated forming doping pockets 106A that are located beneath the source/drain regions 105A. See FIG. 1C of Noda et al. As illustrated, the peak concentration of the doping pockets within Noda et al. is not located substantially at an interface between a strained semiconductor layer and an underlying substrate, as presently claimed.

Applicants further submit that one of ordinary skill in the art would not substitute the halo dopants disclosed in Noda et al. for the carbon that is being implanted to provide a strained material in Xiang et al. Halo dopants, which are utilized to decrease diffusion of source and drain dopants, which provide the charge carriers of a semiconductor device, are far removed from implants that modify the crystalline structure of a semiconductor structure. Applicants submit that the Examiner has failed to provide sufficient reasoning why one of ordinary skill in the art would combine a reference that discloses forming strained semiconductor materials, i.e., Xiang et al., with a reference that discloses a means to reduce diffusion of source and drain dopants, i.e., Noda et al., in a manner that would meet the limitations of Applicants' claims. Specifically, The Examiner has failed to provide reasoning why one of ordinary skill in the art would substitute a dopant species for a halo regions, as taught in Noda et al., with a dopant species to modify the crystal structure of a semiconductor material, as taught in Xiang et al., where the dopant species would block threading defects at the interface of a first strained layer of semiconductor material and a SiGe substrate, as required by Applicants' claims.

KSR International. Co. v. Teleflex, Inc., et al., 550 U.S.____(2007) requires that an Examiner provide "some articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness." (KSR Opinion at p. 14). Remember, an Examiner must

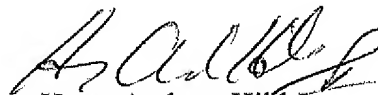
“identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does,” (KSR Opinion at p. 15). And, the Examiner must make “explicit” this rationale of “the apparent reason to combine the known elements in the fashion claimed,” including a detailed explanation of “the effects of demands known to the design community or present in the marketplace” and “the background knowledge possessed by a person having ordinary skill in the art.” (KSR Opinion at p. 14). Anything less than such an explicit analysis may not be sufficient to support a prima facie case of obviousness.

Turning to the AAPA, Applicants note that the AAPA only discloses the existence of threading defects. The AAPA fails to teach or suggest a peak concentration of blocking impurity dopant materials selected from the group consisting of In, Pb, Sb and Sn, in which the implant is located substantially at an interface between a first strained layer of semiconductor material and a SiGe substrate, wherein the blocking impurity dopant materials partially or fully occupy each of the one or more threading dislocations, misfit dislocations or crystal defects at the interface of a first strained layer of semiconductor material and a SiGe substrate, as recited in Claim 1. Further, the AAPA provides no guidance for combining the disclosures of Xiang et al. with Noda et al. to meet Applicants’ claims.

The rejection under 35 U.S.C. § 103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

A handwritten signature in dark ink, appearing to read 'H. A. Hild Jr.', with a stylized flourish at the end.

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